Notice of Allowability	Application No.	Applicant(s)	
	10/051,701	JEON, JIN	
	Examiner	Art Unit	
	Thoi V Duong	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the Response filed 09/04/2003*.
2. ☒ The allowed claim(s) is/are *1-19 and 36-43*.
3. ☐ The drawings filed on _____ are accepted by the Examiner.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.
5. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
   (a) ☐ The translation of the foreign language provisional application has been received.
6. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. **THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

7. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
8. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No. ____.
   (b) ☐ including changes required by the proposed drawing correction filed _____, which has been approved by the Examiner.
   (c) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No. _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the margin according to 37 CFR 1.121(d).

9. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1☒ Notice of References Cited (PTO-892)
2☒ Notice of Draftperson's Patent Drawing Review (PTO-948)
3☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No. _____
4☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5☐ Notice of Informal Patent Application (PTO-152)
6☐ Interview Summary (PTO-413), Paper No._____ .
7☒ Examiner's Amendment/Comment
8☒ Examiner's Statement of Reasons for Allowance
9☐ Other .

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Group I, claims 1-19 and 36-43, in the Response to Restriction Requirement filed September 04, 2003 is acknowledged. The traversal is on the ground(s) that the examination of Group I as product made and Group II (claims 20-35) as process of making will not present an undue burden. This is not found persuasive because the semiconductor layer of Group I can be made by lightly-doped or heavily-doped semiconductor instead of non-doped semiconductor. Because these inventions are distinct the search required for Group I is not required for Group II.

The requirement is still deemed proper and is therefore made FINAL.

Accordingly, claims 1-19 and 36-43 are considered and claims 20-35 are withdrawn from consideration in this office action.

EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Frank Chau (Reg. 34,136) on 12/09/2003.

In the claims: cancel claims 20-35.

Allowable Subject Matter

3. Claims 1-19 and 36-43 are allowed.

The following is an examiner's statement of reasons for allowance: none of the prior art of record fairly suggests or shows all of the limitations as claimed. Specifically,

Re claims 1 and 36, none of the prior art of record discloses, in combination with other limitations as claimed, an LCD panel (as well as a method for manufacturing the same) comprising:

a first insulating interlayer 9 formed on the data pattern and the gate insulating film, the first insulating interlayer having a first contact hole for partially exposing the first electrode, a second contact hole for exposing the gate electrode of a first drive transistor of the peripheral region, and a third contact hole for exposing the second electrode of a second drive transistor of the peripheral region; and

an electrode pattern part formed on the first insulating interlayer, the electrode pattern part including a first electrode pattern in contact with the first electrode of the pixel region through the first contact hole, and a second electrode pattern connecting the partially exposed gate electrode of the first drive transistor with the exposed second electrode of the second drive transistor through the second and third contact holes.

Re claims 10 and 40, none of the prior art of record discloses, in combination with other limitations as claimed, an LCD panel (as well as a method for manufacturing the same) comprising:

a first insulating interlayer formed on the data pattern and the gate insulating film, the first insulating interlayer including a first contact hole for partially exposing the

second electrode, a second contact hole for partially exposing the first electrode of the pixel region, a third contact hole for exposing the gate electrode of a first drive transistor of the peripheral region, and a fourth contact hole for exposing the first/second electrode of a second drive transistor of the peripheral region; and

an electrode pattern part formed on the first insulating interlayer, the electrode 20 pattern part including a first electrode pattern coupled to the second electrode of the pixel region through the first contact hole, a second electrode pattern coupled to the first electrode of the pixel region through the second contact hole, and a third electrode pattern connecting the exposed gate electrode of the first drive transistor with the exposed first/second electrode of the second drive transistor through the third and fourth contact holes.

The most relevant references, USPN 6,261,881 B1 (US'881) and USPN 6,384,818 B1 (US'818) of Yamazaki et al., fail to disclose or suggest such combination. As shown in Figs. 3 and 4, the US'881 discloses a reverse-stagger type TFT CMOS circuit comprising a first drive transistor (P-channel TFT) and a second drive transistor (N-channel TFT) of the peripheral region having contact holes in the insulating interlayer 117 for exposing the source and drain electrodes only. Meanwhile, the US'818 shows in Fig. 8A a CMOS circuit comprising a first drive transistor having a second contact hole for exposing the gate electrode of the first drive transistor and a second drive transistor having a third contact hole for exposing the second electrode of the second drive transistor. However, this circuit is not a reverse-stagger type TFT.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thoi V. Duong whose telephone number is (703) 308-3171. The examiner can normally be reached on Monday-Friday from 8:00 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached at (703) 305-3492.

Thoi Duong

12/09/2003

T. Chowdhury
Primary Examiner